IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please amend claims 1, 5, 11 and 15 in accordance with the following:

1. (CURRENTLY AMENDED) A cache memory system, comprising:

tag memory sections in number n;

cache memory sections in number n, each capable of switching a state between an ordinary state and a lower power consumption state;

consumption power mode control units in number n, individually controlling each cache memory section;

a power control unit which controls switching of a way constitution to either an n-way constitution, in which all the cache memory sections are activated in the ordinary state based on a power mode signal, or a 1-way constitution, in which only one of the cache memory sections is activated in the ordinary state and the remaining cache memory sections are turned into the lower consumption power state, based on a value of an input request address;

a data selector which selects only data read from any one of the cache memory sections when reading the data; and

a data selector control unit which controls the data selector so as to select only data read from the cache memory section corresponding to the value of the request address, in case of the n-way constitution, and to select only data read from the cache memory section in the ordinary state, in case of the 1-way constitution.

2. (PREVIOUSLY PRESENTED) The cache memory system according to claim 1, wherein the power control unit comprises a logic circuit generating a signal for controlling an operation state of each of the cache memory sections, based on the value of the request address and a value of the power mode signal.

3. (PREVIOUSLY PRESENTED) The cache memory system according to claim 1, further comprising:

a tag determination circuit which determines whether or not the address data read from each of the tag memory sections is coincident with the value of the request address; and

a data selector control circuit which controls so as to select any one of data read from each of the cache memory sections based on a determination result of the tag determination circuit, a value of the power mode signal and a control content of the power control unit.

4. (ORIGINAL) The cache memory system according to claim 1, wherein the n cache memory sections correspond to individual n regions divided from one module.

5. (CURRENTLY AMENDED) A cache memory system, comprising:

tag memory sections in number n, each capable of switching a state between an ordinary state and a lower consumption power state;

cache memory sections in number n, each capable of switching a state between the ordinary state and the lower consumption power state;

consumption power mode control units in number n, individually controlling each cache memory section;

a power control unit which controls switching of a way constitution to either an n-way constitution, in which all the tag memory sections and all the cache memory sections are activated in the ordinary state based on a power mode signal, or a 1-way constitution, in which only one tag memory section and only one cache memory section, corresponding to the tag memory section, are activated in the ordinary state and the remaining tag memory sections and cache memory sections are turned into the lower consumption power state, based on a value of an input request address;

a data selector which selects only data read from any one of the cache memory sections when reading the data; and

a data selector control unit which controls the data selector so as to select only data read from the cache memory section corresponding to the value of the request address in case of the n-way constitution and to select only data read from the cache memory section in the ordinary state in case of the 1-way constitution.

6. (PREVIOUSLY PRESENTED) The cache memory system according to claim 5, wherein the power control unit comprises a logic circuit generating a signal controlling an operation state of each of the tag memory sections and each of the cache memory sections, based on the value of the request address and a value of the power mode signal.

7. (PREVIOUSLY PRESENTED) The cache memory system according to claim 5, further comprising:

a tag determination circuit which determines whether or not the address data read from each of the tag memory sections is coincident with the value of the request address; and

a data selector control circuit which controls, so as to select any one of data read from each of the cache memory sections, based on a determination result of the tag determination circuit, a value of the power mode signal and a control content of the power control unit.

8. (PREVIOUSLY PRESENTED) The cache memory system according to claim 5, wherein the data selector control unit comprises:

a tag determination circuit which determines whether or not the address data read from each of the tag memory sections is coincident with the value of the request address; and

a tag determination result invalidation circuit which invalidates a determination result of the tag determination circuit if the address data read from the tag memory section in the lower consumption power state is coincident with the value of the request address.

9. (ORIGINAL) The cache memory system according to claim 5, wherein the n cache memory sections correspond to individual n regions divided from one module.

10. (ORIGINAL) The cache memory system according to claim 5, wherein the n tag memory sections correspond to individual n regions divided from one module.

11. (CURRENTLY AMENDED) A cache memory system, comprising:

tag memory sections in number n connected in parallel;

cache memory sections in number n each capable of switching a state between an ordinary state and a lower consumption power state;

consumption power mode control units in number n, individually controlling each cache memory section;

a power control unit which controls an operation state of each of the cache memory sections so that only one cache memory section, among the cache memory sections, is activated in the ordinary state and the remaining cache memory sections are turned into the lower consumption power state based on a value of an input request address;

a data selector which selects only data read from any one of the cache memory sections

when reading the data; and

a data selector control unit which controls the data selector so as to select only data read from the cache memory section turned into the ordinary state by the power control unit.

12. (PREVIOUSLY PRESENTED) The cache memory system according to claim 11, wherein the power control unit comprises a logic circuit generating a signal for controlling an operation state of each of the cache memory sections based on the value of the request address.

13. (PREVIOUSLY PRESENTED) The cache memory system according to claim 11, wherein the data selector control unit comprises:

a tag determination circuit which determines whether or not the address data read from each of the tag memory sections is coincident with the value of the request address; and

a data selector control circuit which controls so as to select any one of data read from the cache memory sections based on a determination result of the tag determination circuit and a control content of the power control unit.

14. (ORIGINAL) The cache memory system according to claim 11, wherein the n cache memory sections correspond to individual n regions divided from one module.

15. (CURRENTLY AMENDED) A cache memory system, comprising:

tag memory sections in number n, each capable of switching a state between an ordinary state and a lower consumption power state;

cache memory sections in number n, each capable of switching a state between the ordinary state and the lower consumption power state;

consumption power mode control units in number n, individually controlling each cache memory section;

a power control unit which controls an operation state of each of the tag memory sections and each of the cache memory sections so that only one tag memory section and only one cache memory section, corresponding to the tag memory section among the tag memory sections and the cache memory sections, are activated in the ordinary state and the remaining tag memory sections and cache memory sections are turned into the lower consumption power state based on a value of an input request address;

a data selector which selects only data read from any one of the cache memory sections when reading the data; and

a data selector control unit which controls the data selector so as to select only data read from the cache memory section turned into the ordinary state by the power control device.

16. (PREVIOUSLY PRESENTED) The cache memory system according to claim 15, wherein the power control unit is constituted out of a logic circuit generating a signal for controlling an operation state of each of the tag memory sections and each of the cache memory section based on the value of the request address.

17. (PREVIOUSLY PRESENTED) The cache memory system according to claim 15, wherein the data selector control unit comprises:

a tag determination circuit which determines whether or not the address data read from each of the tag memory sections is coincident with the value of the request address; and

a data selector control circuit which controls, so as to select any one of data read from the cache memory sections based on a determination result of the tag determination circuit and a control content of the power control unit.

18. (PREVIOUSLY PRESENTED) The cache memory system according to claim 15, wherein the data selector control unit comprises:

a tag determination circuit which determines whether or not the address data read from each of the tag memory sections is coincident with the value of the request address; and

a tag determination result invalidation circuit which invalidates a determination result of the tag determination circuit if the address data read from the tag memory section in the lower consumption power state is coincident with the value of the request address.

19. (ORIGINAL) The cache memory system according to claim 15, wherein the n cache memory sections correspond to individual n regions divided from one module.

20. (ORIGINAL) The cache memory system according to claim 15, wherein the n tag memory sections correspond to individual n regions divided from one module.